Amendments to the Specification

Please amend the paragraph beginning at line 13 of page 1 as follows:

Conventionally, in a recording and reproduction apparatus, a communication apparatus or the like for digital information, an automatic equalizer for consecutively performing automatic equalization is employed in the way or at the end of a transmission line in order to compensate for deterioration of signals resulting from, ~~by~~ such as, data errors due to characteristics of these apparatuses or the quality of the transmission line.

Please amend the paragraph beginning at line 16 of page 7 as follows:

In recent years, in the digital data reproduction apparatus, the rate ~~speed-up~~ of the data transfer speed is advancing, and the high-speed reproduction has become essential. The increase in the reproduction speed leads to an increase in the frequency of the reference clock included in the digital reproduction signal. This also leads to an increase in the frequency of the operation clock in the analog/digital converter 1 and the automatic equalizer 9. In this way, the high-speed reproduction is directly tied in with the increase in the power consumption. Further, in order to perform high-speed reproduction with stability, it is necessary that the precision of signal processing and a time sufficient for positively performing signal processing are ensured, and the increase in the circuit scale due to an insertion of a delay element which is involved for keeping the number of the arithmetic bits and for keeping the number of bits cannot be avoided. Increasing the circuit scale leads to an increase in the power consumption.

Please amend the paragraph beginning at line 1 of page 10 as follows:

A ~~In a~~ reproduction signal processor in accordance with one aspect ~~of Claim 1~~ of the present invention comprises: ~~comprising:~~ an analog/digital converter for sampling an analog signal, and converting the same into the digital signal; an automatic equalizer for performing an automatic equalization of the digital signal; a phase locked loop for generating a reference clock which coincides with a phase included in the digital signal and reference frequency components; and a frequency divider for generating a frequency-divided clock obtained by performing integral multiplication of the period of the reference clock, and outputting the frequency-divided clock as an operation clock to the analog/digital converter and the automatic equalizer., The ~~the~~

automatic equalizer is composed of: a transversal filter for performing waveform equalization of the digital signal; a straight-line interpolation unit for interpolating the omission of the sampling number due to sampling using the frequency-divided clock in the output of the transversal filter; and a control unit for estimating an equalization target value in accordance with the output of the transversal filter, and controlling a parameter of the transversal filter such that an equalization error which is an error between the equalization target value and the output of the transversal filter becomes minimum.

Please amend the paragraph beginning at line 6 of page 11 as follows:

According to a reproduction signal processor of a second aspect ~~Claim 2~~ of the present invention, in the reproduction signal processor of the first aspect ~~Claim 1~~, the straight-line interpolation unit is composed of: a flip-flop element for performing delay processing of an output equalization signal of the transversal filter for one period of the frequency-divided clock; and an adder for adding a signal after the delay processing and the output equalization signal.

Please amend the paragraph beginning at line 21 of page 11 as follows:

According to a reproduction signal processor of a third aspect ~~Claim 3~~ of the present invention, in the reproduction signal processor of the first aspect ~~Claim 1~~, instead of the straight-line interpolation unit, a high-order interpolation unit for interpolating the omission of the sampling number due to sampling using the frequency-divided clock in the output of the transversal filter is provided.

Please amend the paragraph beginning at line 15 of page 12 as follows:

According to a reproduction signal processor of a fourth aspect ~~Claim 4~~ of the present invention, in the reproduction signal processor of the third aspect ~~Claim 3~~, the high-order interpolation unit is composed of: a flip-flop element for performing delay processing for one period of the frequency-divided clock; plural multipliers for performing weighting of a tap coefficient on a signal after the delay processing; and an adder for adding an output signal of the plural multipliers.